PHASE INDICATION APPARATUS

[0001] This application is a divisional of U.S. Patent Application Serial No. 10/146,689, filed on May 14, 2002, which is a divisional of U.S. Patent Application Serial No. 09/735,858, filed on December 13, 2000, now issued as U.S. Patent No. 6,420,912, which are both incorporated herein by reference.

Field

[0002] Various embodiments may relate generally to voltage-to-current converters, including linear voltage-to-current converters, and phase indication apparatus, such as phase lock loop circuitry..

Background

[0003] Phase lock loop (PLL) circuits and delay lock loop (DLL) circuits are commonly used in integrated circuits today. Example uses for these circuits include clock recovery in communications systems and clock signal alignment in digital systems.

[0004] PLLs and DLLs often incorporate a phase detector and a voltage controlled oscillator (VCO). The VCO generates an output signal with a phase and frequency that is a function of a control voltage. The phase detector measures the phase difference between an input signal and the output signal, and adjusts the control voltage of the VCO. The control voltage to the VCO represents a phase difference, or "phase error" between the input signal and the output signal. When the phase error is large enough, the VCO changes the phase or frequency of the output signal to more closely match that of the input signal.

[0005] Examples of PLLs, DLLs, VCOs, and phase detectors are described in: Ian A. Young, Jeffrey K. Greason, and Keng L. Wong, "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," IEEE Journal of Solid-State Circuits, pp. 1599-1607, Vol. 27, No. 11, Nov. 1992; and Henrik O.

Johansson, "A Simple Precharged CMOS Phase Frequency Detector," IEEE Journal of Solid-State Circuits, pp. 295-299, Vol. 33, No. 2, Feb. 1998.

[0006] The phase detectors described in the above references exhibit a "dead zone" in the phase characteristic at the equilibrium point under certain conditions. The dead zone generates phase jitter in part because the VCO does not change the phase of the output signal when the phase error is within the dead zone. As the operating frequency of integrated circuits increases, PLLs, DLLs, and their associated VCOs and phase detectors are also operating faster, and the size of the dead zone becomes an important factor in the design of circuits.

[0007] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternate phase detectors and circuits that incorporate phase detectors.

Brief Description of the Drawings

Figure 1 shows a phase lock loop;

Figure 2 shows a phase detector;

Figure 3 shows sampling circuit waveforms;

Figure 4 shows a block diagram of a voltage-to-current circuit;

Figure 5 shows a circuit diagram of a voltage-to-current circuit;

Figures 6A-6C show graphical results of a simulation of the circuit of Figure 5; and

Figure 7 shows an integrated circuit having a phase lock loop.

Detailed Description

[0008] The method and apparatus of the various embodiments of the invention may provide a mechanism to convert a voltage to a current. Some embodiments may combine the voltage-to-current circuit with a sampling circuit to implement a phase detector circuit. Two polarities of a differential signal can be sampled, and the voltage difference between the two polarities of the differential

signal may be providd as an input to the voltage-to-current circuit. The voltage-to-current circuit may be a linear circuit that combines two complementary voltage-to-current circuits with a common gate output stage.

[0009] Figure 1 shows a phase lock loop (PLL). PLL 100 may include a phase detector 106, voltage controlled oscillator (VCO) 110, and frequency divider 114. Phase detector 106 may receive an input clock signal on node 102, and a clock signal on node 104. Phase detector 106 may measure a phase difference between signals on nodes 102 and 104, and generate a voltage on node 108 that is a function of the phase difference. VCO 110 may receive the voltage on node 108, and produce an output clock signal on node 112.

[0010] Signals on nodes 102 and 104 can be single-ended or differential signals. For example, the input clock signal on node 102 can include a single signal, or two signals that are complements of each other. Likewise, the signal on node 104 can include a single signal, or two signals that are complements of each other. When a node carries a differential signal, that node may includes multiple physical signal traces. For example, in embodiments where the input clock signal is a differential signal, node 102 includes two physical signal traces to carry the differential signals. In some embodiments, VCO 110 produces a differential clock signal on node 112, and frequency divider 114 produces a differential signal on node 104.

[0011] In some embodiments, VCO 110 produces an output clock signal on node 112 that has a frequency other than the frequency of the input clock signal on node 102. For example, in some embodiments, PLL 100 is included in a microprocessor having an internal operating frequency higher than an external clock frequency. In these embodiments, PLL 100 can generate an output clock signal at a greater frequency than an input clock signal, but with matching phase.

[0012] In the embodiment shown in Figure 1, VCO 110 may produce an output clock signal having a frequency higher than the input clock frequency, and frequency divider 114 divides the output clock signal on node 112 to produce a frequency divided signal on node 104. In some embodiments, VCO 110 may

produce an output clock signal at the same frequency as the input clock signal, and frequency divider 114 is not included in PLL 100. For ease of explanation, the remainder of this description describes PLLs, phase detectors, and other circuits operating with signals of the same frequency.

[0013] Figure 2 shows a phase detector. Phase detector 200 may include sampling circuit 210, voltage-to-current circuit 230, and capacitor 250. Sampling circuit 210 may include switches 212 and 214 controlled by a signal on node 202. In the embodiment of Figure 2, the signal on node 202 is labeled "CLOCK1." CLOCK1 is one of two signals input to sampling circuit 210. The other signal input to sampling circuit 210 may be a differential signal consisting of two physical signals received on nodes 204 and 206 that are labeled "CLOCK2+" and CLOCK2-," respectively. Taken together, CLOCK2+ and CLOCK2- represent a single signal represented by the label "CLOCK2."

[0014] CLOCK1 and CLOCK2 correspond to signals on nodes 102 and 104 in Figure 1. For example, in some embodiments, CLOCK1 corresponds to the input clock signal on node 102 (Figure 1), and CLOCK2 corresponds to the clock signal on node 104 (Figure 1). In these embodiments, frequency divider 114 (Figure 1) produces a differential signal on node 104. In other embodiments, CLOCK2 corresponds to the input clock signal on node 102, and CLOCK1 corresponds to the clock signal on node 104. In these embodiments, the input clock signal received on node 102 is a differential signal.

[0015] Sampling circuit 210 may sample voltage values of differential signal CLOCK2 at transition points of CLOCK1, and produce a voltage differential (V_{dif}) between nodes 220 and 222. V_{dif} may represent a phase error between CLOCK1 and CLOCK2. Sampling circuit 210 can be implemented using known techniques for sampling signals.

[0016] Voltage-to-current circuit 230 may receive V_{dif} on nodes 220 and 222 and produces a current on node 240. The current on node 240 may charge and discharge capacitor 250 to produce a voltage for controlling a VCO, such as VCO 110 (Figure 1). Voltage-to-current circuit 230 may be a linear circuit that produces

a current on node 240 without a dead zone, or with a very small dead zone. When V_{dif} is positive, voltage-to-current circuit 230 may source an output current to charge capacitor 250 to a higher voltage. In contrast, when V_{dif} is negative, voltage-to-current circuit 230 may sink an output current to discharge capacitor 250 to a lower voltage.

[0017] Figure 3 shows sampling circuit waveforms for signals CLOCK1 and CLOCK2 of Figure 2. CLOCK1 is represented by waveform 306, CLOCK2+ is represented by waveform 304, and CLOCK2- is represented by waveform 302. CLOCK2+ and CLOCK2- are sampled at transition points of CLOCK1. This is shown at times 310 and 320 in Figure 3. In the embodiment of Figure 3, the transition point is the rising edge of CLOCK1. In other embodiments, the transition is the falling edge of CLOCK1.

[0018] At time 310, CLOCK2 is sampled and V_{dif} exists between points 312 and 314. At time 320, CLOCK2 is again sampled and V_{dif} exists between points 322 and 324. As a result of V_{dif}, voltage-to-current circuit 230 (Figure 2) may change a control voltage for a VCO, which in turn may modify the phase of either CLOCK1 or CLOCK2 to reduce the phase error.

[0019] Figure 4 shows a block diagram of a voltage-to-current circuit. Voltage-to-current circuit 230 may include NMOS-input voltage-to-current (V-I) converter 402, PMOS-input V-I converter 404, and output stage 406. Both NMOS-input V-I converter 402 and PMOS-input V-I converter 404 may receive V_{dif} on nodes 220 and 222. When V_{dif} is positive, NMOS-input V-I converter 402 may source current 420 on node 408, and PMOS-input V-I converter 404 may not contribute to the output current. Current 420 is labeled I_{ON} in Figure 4. When V_{dif} is negative, NMOS-input V-I converter 402 may not contribute to the output current, and PMOS-input V-I converter 404 may sink current 422 on node 410. Current 422 is labeled I_{OP} in Figure 4.

[0020] Output stage 406 can combine currents 420 and 422 to produce output current 424, labeled I_O in Figure 4. Output stage 406 may reduce the sensitivity of the output current for different output voltages.

[0021] Figure 5 shows a circuit diagram of a voltage-to-current (V-I) circuit. V-I circuit 500 may include transconductance amplifiers 520 and 540, current mirrors 510 and 530, and output stage 406. Transconductance amplifier 520 and current mirror 510, taken together, may represent one embodiment of NMOS-input V-I converter 402 (Figure 4). Likewise, transconductance amplifier 540 and current mirror 530, taken together, may represent one embodiment of PMOS-input V-I converter 404 (Figure 4). Each of these circuits may be coupled between upper power supply node 502 and lower power supply node 504.

[0022] Transconductance amplifier 520 may include n-channel input transistors 522 and 524. N-channel input transistors 522 and 524 are shown as n-channel metal oxide semiconductor field effect transistors (MOSFETs), and represent any type of transistor having an n-type channel. The terms "NMOS" and "n-channel" are used herein to describe such a transistor. Likewise, the terms "PMOS" and "p-channel" are used herein to describe transistors having p-type channels. Transconductance amplifiers of the type shown as transconductance amplifier 520 in Figure 5 are described in: S. C. Huang and M. Ismail, "Linear Tunable COMFET Transconductor," Electronics Letters, pp. 459-461, Vol. 29, No. 5, Mar. 1993. Transconductance amplifiers 520 and 540 may include bias nodes to receive bias voltages VB1 and VB2, respectively. In some embodiments, VB1 and VB2 are adjustable control voltages of the V-I converters to reduce process, temperature, and power supply variations.

[0023] Current mirror 510 may include p-channel transistors 512 and 514. P-channel transistor 512 may be diode connected, and have a gate coupled to the gate of p-channel transistor 514. The source-to-drain current in transistors 512 and 514 may be, therefore, substantially equal. As V_{dif} changes, the gate voltage on n-channel transistors 522 and 524 may also change. As the gate voltage changes, the drain-to-source current in transistors 522 and 524 may change. The constant current in current mirror 510, and the varying currents in the n-channel input transistors of transconductance amplifier 520 may result in a varying current 420. When V_{dif} is positive, current 420 may flow in the direction of the arrow shown in Figure 5.

When V_{dif} is negative, current 420 may not flow. This is due in part to the operation of output stage 406, discussed in more detail below.

[0024] Transconductance amplifier 540 may be a complementary version of transconductance amplifier 520. Transconductance amplifier 540 may include p-channel input transistors 542 and 544. Current mirror 530 may include n-channel transistors 532 and 534. N-channel transistor 532 may be a diode connected transistor having a gate coupled in common with a gate of n-channel transistor 534. As a result, drain-to-source currents in transistors 532 and 534 may be substantially equal. As V_{dif} on nodes 220 and 222 varies, so may the source-to-drain current in p-channel input transistors 542 and 544. As a result, current 422 may be produced. When V_{dif} is negative, current 422 may flow in the direction shown by the arrow in Figure 5. When V_{dif} is positive, current 422 may not flow, in part because of the operation of output stage 406.

[0025] Output stage 406 may be a common gate output stage having two pairs of complementary transistors with gates coupled in common. For example, p-channel transistor 556 and n-channel transistor 558 may form a series connected complementary pair coupled between the output node of the NMOS-input V-I converter and the output node of the PMOS-input V-I converter. A junction between transistors 556 and 558 may form output node 240 of V-I converter 500. P-channel transistor 550 and n-channel transistor 552 may form a series connected complementary pair of transistor coupled between the upper power supply node and the lower power supply node. Gates of transistors within output stage 406 may all be coupled in common with node 554 formed at the junction between p-channel transistor 550 and n-channel transistor 552. In this manner, transistors 550 and 552 may form a bias circuit to provide a gate bias for transistors 556 and 558. In other embodiments, different bias circuits are used to bias transistors 556 and 558.

[0026] In operation, when V_{dif} is positive, p-channel transistor 556 may be on and n-channel transistor 558 may be off. This allows current 420 to flow as current 424 on output node 240. When V_{dif} is negative, n-channel transistor 558 may be on and p-channel transistor 556 may be off, allowing current 424 to flow in

the direction opposite the arrow shown in Figure 5 to discharge capacitance on output node 240. The operation of the V-I converter 500 has been simulated in a 0.16 micron complementary metal-oxide semiconductor (CMOS) process. Graphical results from the simulation are shown and described with reference to Figures 6A-6C.

[0027] Figures 6A-6C show graphical results of a simulation of the circuit of Figure 5. Figure 6A shows output current 424 (Figure 5) as a function of input differential voltage V_{dif}. Graph 600 shows the differential mode gain at curve 610. Curve 610 represents the differential mode gain of V-I converter 500, as well as the individual differential mode gains of the NMOS-input and PMOS-input converters without output stage 406. The output current various substantially monotonically from -0.44 to 0.44 mA as the input differential voltage increases from -1.5 volts to 1.5 volts. The output current of V-I converter 500 (Figure 5) utilizes the NMOS-input V-I converter while the input differential voltage is positive, and utilizes the PMOS-input V-I converter while the input differential voltage is negative. This complementary operation exhibits a large input differential voltage range, which may be applied to circuits that can benefit from a linear V-I relationship.

[0028] Figure 6B shows output current 424 (Figure 5) as a function of input common mode voltage. Graph 620 shows curves 622, 624, and 626. Curve 622 represents output current 424 of V-I converter 500. Curves 624 and 626 represent the output currents of the NMOS-input and PMOS-input V-I converters, respectively, when operating without each other and without output stage 406. Output current 424 varies within -6uA to 4uA as the two input signals increase from 0 volts to 1.5 volts, as shown by curve 622. This common mode variation is generally smaller than variations of the individual NMOS-input and PMOS-input V-I converters. This is shown by the contrast between curves 622 and 624, and also by the contrast between curves 622 and 626.

[0029] Figure 6C shows the effect of the output voltage on the output current. Graph 630 shows curves 632, 634, and 636. Curve 632 represents output current 424 (Figure 5) of V-I converter 500. Curves 634 and 636 represent the

output currents of the NMOS-input and PMOS-input V-I converters, respectively, when operating without each other and without output stage 406. The data for curve 632 was generated with V_{dif} set to zero, and each of input nodes 220 and 222 biased at 0.75 volts. Output current 424 is close to zero when the output voltage is in the range of 0.5 volts to 1.0 volts. This is in contrast to the behavior of the NMOS-input and PMOS-input V-I converters operating without output stage 406. This is shown by the contrast between curves 632 and 634, and also by the contrast between curves 632 and 636.

[0030] Figure 7 shows an integrated circuit having a phase lock loop. Integrated circuit 700 may include PLL 702 and sequential elements 706, 708, and 710. PLL 702 may receive an external clock on node 722 and produce an internal clock on node 704. PLL 702 can be any PLL embodiment disclosed herein. For example, PLL 702 can incorporate phase detector 200 (Figure 2), and V-I circuit 500 (Figure 5). Sequential elements 706, 708, and 710 are shown as D-type flip-flops clocked by the internal clock on node 704, but this is not a limitation on embodiments of the present invention. For example, PLL 702 can create a clock signal that drives latches, flip-flops other than D-type flip-flops, or any other type of sequential element.

[0031] Sequential element 706 may receive external data from node 720, and sequential element 710 may drive external data on node 724. PLL 702 may substantially align the phase of the clocks on nodes 722 and 704 such that data on node 720 is received properly by sequential element 706.

[0032] Integrated circuit 700 is shown having a phase lock loop generating a clock to operate digital circuits. This can be useful in many different types of digital integrated circuits. Examples include, but are not limited to, processors such as microprocessors and digital signal processors, microcontrollers, sequential memories incorporating static random access memory (SRAM) or dynamic random access memory (DRAM), or the like. Integrated circuit 700 can also be an analog integrated circuit, such as a communications device that utilizes PLL 702 to recover a clock from data.

[0033] The accompanying drawings that form a part hereof show by way of illustration, and not of limitation, specific embodiments in which the subject matter may be practiced. The embodiments illustrated are described in sufficient detail to enable those skilled in the art to practice the teachings disclosed herein. Other embodiments may be utilized and derived therefrom, such that structural and logical substitutions and changes may be made without departing from the scope of this disclosure. This Detailed Description, therefore, is not to be taken in a limiting sense, and the scope of various embodiments is defined only by the appended claims, along with the full range of equivalents to which such claims are entitled.

[0034] Such embodiments of the inventive subject matter may be referred to herein, individually and/or collectively, by the term "invention" merely for convenience and without intending to voluntarily limit the scope of this application to any single invention or inventive concept if more than one is in fact disclosed. Thus, although specific embodiments have been illustrated and described herein, it should be appreciated that any arrangement calculated to achieve the same purpose may be substituted for the specific embodiments shown. This disclosure is intended to cover any and all adaptations or variations of various embodiments. Combinations of the above embodiments, and other embodiments not specifically described herein, will be apparent to those of skill in the art upon reviewing the above description.

[0035] The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby

incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.